REMARKS

Claims 1-14 were examined and reported in the Office Action. Claims 13 and 14 are allowed. Claims 1 and 12 are rejected. Claim 1 is amended. Claims 1-14 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 102(b)

It is asserted in the Office Action that claim 1 is rejected under 35 U.S.C. § 102(b), as being anticipated by U. S. Patent No. 5,764,572 issued to Hammick ("Hammick"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131, "'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's amended claim 1 contains the limitations of "[a] semiconductor memory device, comprising: a first cell array including a plurality of unit cells to be selected by an address signal; a sense amplifying unit for sensing and amplifying voltage level of a bit line connected to the plurality of the unit cells; a switching unit for connecting or disconnecting the sense amplifying unit to the bit line; and a sense amplifying connection unit for controlling the switching unit for connecting or disconnecting the sense amplifying unit to the first cell array by increasing or decreasing an amount of current throughout the switching unit in response to the address signal, wherein the sense amplifying connection unit temporarily disconnects the sense amplifying unit to the first cell array for the sensing and the amplifying

voltage level and reconnects the sense amplifying unit to the first cell array by stepwise increasing the amount of current."

Applicant first notes that in general, a sense amplifier is included in a semiconductor memory device for sensing and amplifying a potential difference between bit lines. For increasing an operational speed of the sense amplifier, the sense amplifier is temporarily disconnected to a memory cell array during the sense amplifying operation. Then, the sense amplifier is reconnected to the memory cell array. At this time, i.e., when reconnecting the sense amplifier to the memory cell array, bit line noise is generated. Therefore, the semiconductor memory device is transiently unstable at that moment. This problem is described in Applicant's background section.

Applicant's claimed invention solves the aforementioned problem by providing the semiconductor memory device with the sense amplifying connection unit for controlling the switching unit for connecting or disconnecting the sense amplifying unit to the first cell array by increasing or decreasing an amount of current throughout the switching unit in response to the address signal. The sense amplifying connection unit temporarily disconnects the sense amplifying unit to the first cell array for the sensing and the amplifying voltage level and reconnects the sense amplifying unit to the first cell array by stepwise increasing the amount of current.

Hammick discloses a sensing device for an integrated circuit memory device having a dynamic sense amplifier suitable for use in these memory. Hammick, however, neither discloses nor suggests a sense amplifying connection unit that stepwise increases the amount of current for reconnecting the sense amplifying unit to a memory cell array. Moreover, Hammick does not teach, disclose or suggest temporarily disconnecting the sense amplifying unit to the memory cell array for increasing the operational speed.

Therefore, since Hammick does not disclose, teach or suggest all of Applicant's amended claim 1 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(b) has not been adequately set forth relative to Hammick. Thus, Applicant's amended claim 1 is not anticipated by Hammick.

Accordingly, withdrawal of the 35 U.S.C. § 102(b) rejection for claim 1 is respectfully requested.

II. 35 U.S.C. § 103(a)

It is asserted in the Office Action that claim 12 is rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Hammick in view of U.S Patent No. 6,008,689 issued to Au et al. ("Au"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." "*All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's claim 12 directly depends on amended claim 1. Applicant has addressed Hammick regarding amended claim 1 above in section I.

Au discloses a switch circuit having a switch and a body grabbing circuit. The switch includes a first and second transistor. The first transistor has a body and is coupled to the second transistor in parallel to form a common source and a common drain. The common source defines an input node and the common drain defines an output node. The first body grabbing circuit is connected to the body of the first transistor. The first body grabbing circuit is arranged to connect the body of the first

transistor to the input node when the first and second transistors receive a turn-on voltage signal such that a body effect is eliminated in the first transistor. Au, however, does not teach, disclose or suggest "the sense amplifying connection unit temporarily disconnects the sense amplifying unit to the first cell array for the sensing and the amplifying voltage level and reconnects the sense amplifying unit to the first cell array by stepwise increasing the amount of current."

Therefore, even if Hammick were combined with Au, the resulting invention would still not include all of Applicant's claimed limitations. And, therefore, there would be no motivation to combine Hammick with Au. Thus, Applicant's amended claim 1 is not obvious over Hammick in view of Au since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claim that directly depends from amended claim 1, namely claim 12, would also not be obvious over Hammick in view of Au for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claim 12 is respectfully requested.

III. Allowable Subject Matter

Applicant also notes with appreciation the Examiner's assertion that claims 13 and 14 are allowable over the prior art of record.

Applicant also notes with appreciation the Examiner's assertion that claims 2-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully asserts that claims 1-14, as they now stand, are allowable for the reasons given above.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-14 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: November 11, 2004

By: _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on November 11, 2004.

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Jean Svoboda